REMARKS

Claims 37 and 38 have been added. Claim 37 is substantially similar to originally filed claim 27 and claim 38 is identical to claim 37 except that it is written in structure format rather than method format. Please charge any costs to Deposit Account No 20-0668.

Claims 29 to 36, while withdrawn, are retained since they represent interfering subject matter and should be handled in this application on a special basis since the relate to interfering subject matter and for reasons stated hereinbelow.

Claims 21 to 25, 27 and 28 were rejected under 35 U.S.C. 102(b) as being anticipated by Cotues et al. (U>S. 5,239,447). The rejection is respectfully traversed.

Claim 21, from which claims 22 to 25, 27 and 28 depend require, among other features, "electrically connecting said at least one electrical *terminal on said at least one edge surface of said integrated circuit package* to said top surface of said printed circuit board at an acute angle with said top surface of said printed circuit board". No such feature is taught or even remotely suggested by Cotues et al. Note with respect to figures 4 and 5 of Cotues et al. that the terminal is not on the edge surface of the package but rather on a major surface. The surface 76 of Cotues et al. is specifically stated at column 5, lines 47ff to be "a dielectric layer such as a silicon dioxide layer or other dielectric coating on a silicon electronic device 40'. It follow that the edge surface of the integrated circuit package of Cotues et al. is not an electrical terminal as required by claim 21 and is not electrically connected to the circuit board.

Claims 22 to 25, 27 and 28 depend form claim 21 and therefore define patentably over Cotues et al. for at least the reasons set forth above with reference to claim 21.

In addition, claim 22 further limits claim 21 by requiring the step of electrically and perpendicularly connecting at least two integrated circuit packages to the circuit board. No such combination is taught or suggested by Cotues et al..

Claim 23 further limits claim 21 by requiring the step of disposing a solder ball between the side surface terminal of the integrated circuit package and the top of the circuit board. No such combination is taught or suggested by Cotues et al.

Claim 25 further limits claim 21 by requiring the step of integrally attaching at least three tabs to said circuit board. No such combination is taught or suggested by Cotues et al.

Claim 27 further limits claim 21 by requiring that the integrated circuit package be further defined as being connected at an acute angle between 30 and less than 90 degrees to the circuit board. No such feature is is taught or suggested by Cotues et al. either alone or in the combination as claimed..

Claim 28 further limits claim 21 by requiring that the at least one edge surface is four edge surfaces, each of the four edge surfaces disposed between the major surfaces to form a closed package with the major surfaces. No such combination is taught or suggested by Cotues et al.

Claims 37 and 38 are patterned after claim 27 and define patentably over Cotues et al. for the reasons presented above with reference to claim 27.

With reference to the proposed interference, among the inventive features are (1), the fact that the connection between the integrated circuit and the circuit board is at an acute angle and provided at the chip end surface and (2) that the acute angle be between 30 and less than 90 degrees. While the Rinne disclosure does not appear to teach

connection from an edge of the integrated circuit as defined in the claims of the subject application, the claims of Rinne can be said to cover such feature.

In order to avoid the present issue at this time with regard to claims 29 to 36 previously copied from Rinne, the prior arguments will be held in abeyance subject to declaration of an interference on the basis of the arguments presented hereinbelow and will be advanced in connection with an interference, if ultimately declared.

Reference will initially be directed to claim 1 of Rinne.wherein two microelectronic substrates are provided with the second microelectronic substrate oriented at an acute angle relative to the first microelectronic substrate. Claim 1 of Rinne further requires solder bumps between the first and second microelectronic substrates, adjacent an edge of the second substrate. There is no limitation as to where the solder bumps are located and, therefore, though the solder bumps of Rinne are shown to be on the edge of the major surface, the claim is not so limiting and reads on the solder bumps being on the edge surface as initially claimed in claim 21 of the subject application. Rinne further requires that the solder bumps be confined to within the edge of the second microelectronic substrate, this also reading of the edge surface of initially filed claim 21 of the subject application.

It follows from the above analysis that claim 1 of Rinne is readable on the invention originally claimed in claim 21 of the subject application.

A proposed count would be claim 21 as presented above, this claim being for the same invention as claim 1 of Rinne.

Since the Rinne file contains a restriction requirement in that application, in the event a divisional application was filed by Rinne, it is requested that an interference also be declared with such application.

In view of the above remarks, favorable reconsideration and declaration of an interference and/or interferences as indicated above are respectfully requested.

Respectfully submitted,

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